REMARKS

Applicant notes with appreciate the finding that claims 5-7, 9-11, 17-19 and 21-23 would be allowable if rewritten in independent form. New claims 26-31 correspond to allowable claims 9-11 and 21-23, with the addition of the subject matter of claim 2 as required by the examiner in the telephone interview, and should thus be allowable. The subject matter of claims 5 and 17 and of intervening claims have been incorporated into the base claims 1 and 13, so claims 1 and 13 should be allowable.

The claims have been amended to expedite issuance. However, for the following reasons, it is submitted that the unamended claims should have been allowed, and applicant reserves the right to file those claims in a continuation application.

Distribution of the frame clock in accordance with the present invention is generally discussed in the specification from the bottom of page 11 through page 16. In accordance with the invention, the frame clock is propagated from a master switch to downstream switches and then from output switches to input switches. In particular, as discussed at the bottom of page 13, it is significant that the propagation of the frame clock match the data distribution between the switches so that, as data signals are delayed, they remain properly aligned to the frame clock

In response to Applicants arguments that there is no suggestion in the cited Collins reference that a clock be propagated to downstream switches and then from output switches to input switches, the Examiner has responded that "This argument is not persuasive because how the clock is distributed from the master to the slave is depending how the switches in the digital cross connect are arranged. The clock can be propagated in different directions so that all the switches in the digital cross connect are synchronized."

First, the undersigned fails to see how a statement that a clock can be propagated in different directions suggests the specific propagation claimed, propagation from a master switch to downstream switches and from output switches to input switches. In fact, such propagation is explicitly not shown in Collins. The only reference to clock distribution that the undersigned has found in the detailed description of Collins is at column 6, lines 46-48. As illustrated in Fig. 3,

the signal from clock 30 is distributed on a timing distribution bus. That bus leads directly to various control stores and inlet and outlet memories in the system. There is no suggestion that the clock propagate from a master switch to downstream switches and from output switches to input switches.

There is no suggestion in Collins of propagating a clock from stage to stage, and particularly such that the propagation matches data distribution. In fact, by using a common timing distribution bus from the clock 30 in Fig. 3 of Collins, the clock signal would be distributed simultaneously to all elements of the circuit without regard to the distribution of data.

With respect to claims 4 and 16, the Examiner has suggested that the original claims "do not claim using those bytes as a mechanism for propagating a frame clock through plural switching stages." Although it is believed that the feature was explicitly claimed by the combination of claims 4 and 16 with their respective base claims 1 and 13, claims 4 and 16 have now been amended to more clearly recite that feature.

CONCLUSION

In view of the above amendments and remarks, it is believed that all claims are in co7ndition for allowance, and it is respectfully requested that the application be passed to issue. If the Examiner feels that a telephone conference would expedite prosecution of this case, the Examiner is invited to call the undersigned.

Respectfully submitted,

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